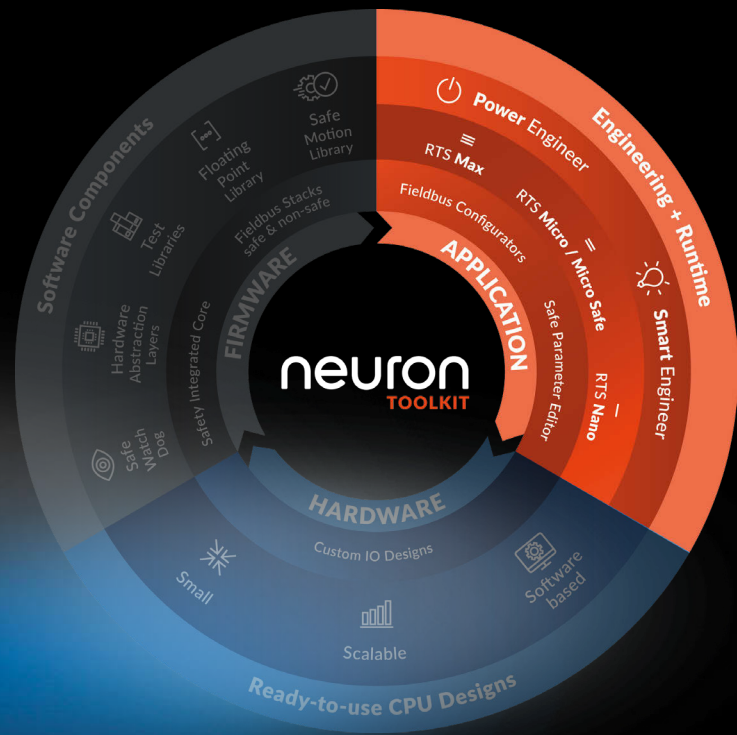


RTS micro



Summary

To build the bridge between our Engineering Tools and the PLC hardware Neuron also offers a variety of runtimes. Neuron RTS safe is a runtime system for execution of standard programs on embedded micro controllers.

Main benefits at one glance

It is hardware independent and OS agnostic and can also be operated bare metal. A data exchange server allows integration of fieldbus protocols and custom add-ons.



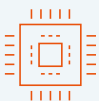
Running on target



Easy to integrate into new and existing systems



Flexible and highly scalable



Open connectivity and extensive usability for plug-in interfaces and system services



Virtualization from the controller to the cloud

Small footprint: executable on small hardware

Easy integration with custom hardware for single and dual channel architectures

Hardware independence and scalable performance from micro controllers to ARM processors

Can be containerized to run as virtual PLC

Extensible through API:

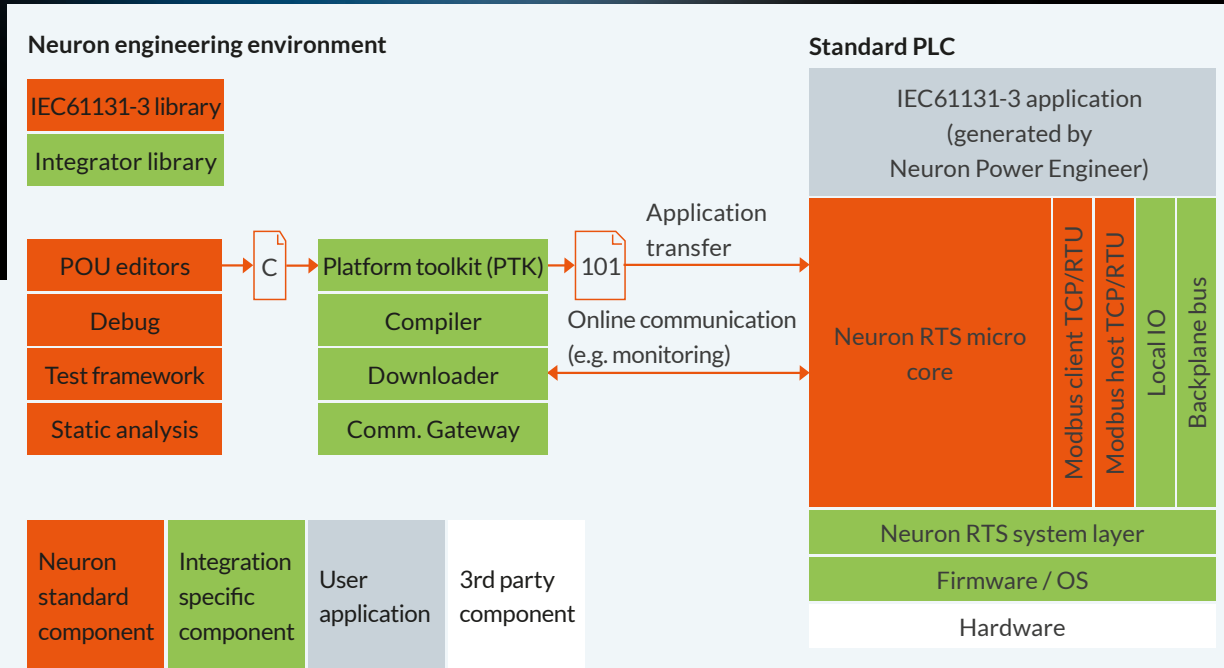
- Integrator can add easily additional functionality via add-on-concept
- Integrator can interact with the system via an API

Additional custom fieldbus solutions can be integrated

Compatibility of interfaces between data exchange layer and data exchange server to minimize integration efforts of OEM extension into both Neuron runtime families

Your Solution Partner for Functional Safety, Engineering Tools & Runtimes

Architecture



Specifications

Multi-tasking runtime for non-safe PLC programs created with Neuron Power or Smart Engineer

Data exchange server for connection between variables in the PLC runtime and safe or non-safe fieldbus systems, data mapping configured at engineering time, protection mechanism to ensure freedom from interference of non-safe communication

Modbus client and server included

Shared Memory interface for I/O connection with custom specific mapping of global variables

No built-in application size limits

Fast cycle times down to 250 μ s

Designed for μ -controller architectures (Cortex-M, Cortex-A)

Features can be tailored to minimize resource consumption

Extensible by the integrator

Small Footprint (32kB ROM and 8kB RAM for runtime core)